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loop and queue and registers

Search

☐ Check to search within this result set**Results Key:****JNL** = Journal or Magazine   **CNF** = Conference   **STD** = Standard**1 Evaluating the use of register queues in software pipelined loops**

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Smelyanskiy, M.; Tyson, G.S.; Davidson, E.S.;

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Pages: 3 - 12[\[Abstract\]](#)   [\[PDF Full-Text \(940 KB\)\]](#)   **IEEE CNF****3 Evaluating the use of register queues in software pipelined loops**

Tyson, G.S.; Smelyanskiy, M.; Davidson, E.S.;

Computers, IEEE Transactions on , Volume: 50 , Issue: 8 , Aug. 2001  
Pages: 769 - 783[\[Abstract\]](#)   [\[PDF Full-Text \(3240 KB\)\]](#)   **IEEE JNL****4 Partitioned schedules for clustered VLIW architectures**

Fernandes, M.M.; Llosa, J.; Topham, N.;

Parallel Processing Symposium, 1998. 1998 IPPS/SPDP. Proceedings of the Fifteenth Merged International...and Symposium on Parallel and Distributed Processing 1998 , 30 March-3 April 1998  
Pages: 386 - 391

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**5 A model for the high-level description and simulation of VLSI networks**  
*van der Hoeven, A.J.; de Lange, A.A.J.; Deprettere, E.F.; Dewilde, P.M.;*  
Micro, IEEE , Volume: 10 , Issue: 4 , Aug. 1990  
Pages:41 - 48

[\[Abstract\]](#) [\[PDF Full-Text \(504 KB\)\]](#) **IEEE JNL**

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**6 A comparison of superscalar and decoupled access/execute architectures**  
*Farrens, M.K.; Ng, P.; Nico, P.;*  
Microarchitecture, 1993. Proceedings of the 26th Annual International Symposium , 1-3 Dec. 1993  
Pages:100 - 103

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